Claims

1. A multi-ported orthogonal data memory (16) for effecting a corner-turning function, where for example data input as a sequence of bit-parallel word-serial data transfers are converted to data output in a bit-serial, word-parallel fashion; the memory (16) being arranged to transfer data words comprising a plurality of data items and comprising:

a plurality of data memory cells (36) arranged in the form of a matrix having rows and columns, and a plurality of groups (A, B, C, D) of memory cells (36) within the matrix, each group being defined across multiple rows and columns and being individually addressable to effect transfer of a data word thereto; and

enabling means having dedicated strobe connections (SDTRW, PDTEN) to each of the plurality of groups (A, B, C, D) of memory cells (36) and being arranged to enable selected ones of the plurality of groups (A, B, C, D) of memory cells (36) to read data present at their inputs or to write stored data to their outputs in a single transfer operation.

2. A memory (16) according to Claim 1, wherein each of the groups (A, B, C, D) of memory cells is specified according to its use in transferring the data items of the data word to or from the matrix to effect the corner-turning function.

3. A memory (16) according to Claim 1 or 2, wherein the enabling means comprises selection means for selecting the current size of the data items in the data word and configuring the enabling means to operate with the selected current size of data items.

4. A memory (16) according to Claim 3, wherein the number of different groups (A, B, C, D) of memory cells provided within the matrix equals the number of different sizes of data items which can be handled by the memory.

5. A memory (16) according to Claim 3 or 4, wherein each item of the data word being transferred is an integer power-of-two multiple of eight bits.

6. A memory (16) according to any preceding Claim 5, wherein the memory is arranged to operate with different types of data words, each type comprising 64, 32, 16 or 8-bit data items.

7. A memory (16) according to any preceding claim, wherein the enabling means is arranged to enable a selected group (A, B, C, D) as determined by the size of the data items being transferred.

8. A memory (16) according to Claim 7, wherein the enabling means is arranged to enable a selected group (A, B, C, D) upon a set of logic conditions becoming true, the logic conditions being determined from a current selected row of the matrix and the size of the items being transferred.

9. A memory (16) according to any preceding claim, wherein the enabling means comprises a pointer in a shift register (38) for determining which rows of the matrix are to be enabled for talking part in the data transfer of all of the data items of the data word.

10. A memory (16) according to Claim 9, wherein the pointer in the shift register (38) is configured to be operable in a plurality of different modes (D8, D16, D32, D64), each mode corresponding to a possible size of the data item being transferred, the pointer being configured within a single instruction to advance by a predetermined number of bit positions as determined by the current mode thereby indicating which rows of the matrix are to be enabled to facilitate transfer of the whole of the data word to or from the matrix.

11. A memory (16) according to any of Claims 9 to 11, further comprising means for storing information relating to a faulty row in the matrix and wherein the shifting word pointer register (38) is arranged to be controlled to skip the faulty row in the matrix and instead point to otherwise redundant additional row of the matrix.

12. A memory (16) according to any of Claims 9 to 11, further comprising means for converting the current position of the row pointer in the shift register (38) to one or more row select logic signals.

13. A memory (16) according to Claim 12, further comprising a hard-wired backward propagation network for determining, from the bit position of the pointer and the size of the current data items, the rows of the matrix that are to be enabled for the data transfer.

14. A memory (16) according to any preceding claim, wherein the enabling means comprises byte column determining means for enabling a specific group of byte column locations of the matrix within a selected word row to be enabled for transferring an item of the data word across a word port of the memory.

15. A memory (16) according to Claim 14, wherein the byte column determining means comprises a table specifying the relationship between the plurality of different groups of memory cells and their respective memory cell locations in the matrix.

16. A memory (16) according to any preceding claim, wherein the enabling means comprises bit column determining means for enabling a specific group of bit column locations of the matrix within a selected word row to be enabled for transferring a bit of an item of the data word across a bit port of the memory.

17. A memory (16) according to Claim 16, wherein the bit column determining means comprises a table specifying the relationship between the plurality of different groups of memory cells and their respective memory cell locations in the matrix.

18. A memory (16) according to any preceding claim, wherein the locations of the memory cells of each group form a repeating pattern when viewed as a matrix.

19. A memory (16) according to any preceding claim, further comprising a load register (42) arranged to retain temporarily bit-serial word parallel data transferred to and from the matrix of memory cells (36) across a bit port of the memory.

20. A memory (16) according to any preceding claim, further comprising a first masking register (44) arranged to mask bits of the data to be read out of the matrix of memory cells (36) via a bit port of the memory.

21. A memory (16) according to any preceding claim, further comprising a second masking register (46) arranged to mask bits of the data to be input to the matrix of memory cells via a bit port of the memory.

22. A multi-ported orthogonal data memory (16) for effecting a data corner-turning function between a plurality of SIMD associative processors and location addressable data store, the memory (16) being arranged to transfer data words comprising a plurality of data items across a word port for the data store and transfer data bits across a bit port for the SIMD associative processors, the memory comprising:

a plurality of data memory cells arranged in the form of a matrix having rows and columns, and a plurality of groups of memory cells within the matrix, each group being defined across multiple rows and columns and being individually addressable to effect transfer of a data word thereto; and

enabling means having dedicated strobe connections to each of the plurality of groups of memory cells and being arranged to enable selected ones of the plurality of groups of memory cells to transfer data items via the word port or bit data via the bit port in a single transfer operation.

23. A combination of a memory (16) as described in any preceding claim and a plurality of SIMD associative processors (12).